C256

Uncooled Thermal Imaging Module

Product Manual

V1.0.0

Revision History

Version	Date	Comments
V1.0.0	2024-07	Initial Release

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1.Product Overview

The C256 uncooled thermal imaging modules are designed for the application fields which require compactness and low power consumption. They can be applied in industries, electric power systems, safety & surveillance and machine vision for its reduction in SWaP, simultaneous image and temperature output, multiple lens choices and compatibility.

2.Lens Options

Table2.1 Optional Lenses

Array Format	E.F.L./F#	Lens Type	FOV H×V	IFOV
256×192	3.2mmF1.1	Athermal	56°×42.2°	3.82mrad
	7mmF1.0		24.8°×18.7°	1.69mrad

3.Product Performance Specifications

Table 3.1 Product Performance Specification

Model	C256
Performance Indicators	
Detector Type	VOx Uncooled IRFPA
Resolution	256×192
Pixel Pitch	12μm
Frame Rate	25Hz
Spectral Range	8～14μm
NETD	≤50mK@25℃, F#1.0
Image Adjustment	
Brightness&Contrast Adjustment	Manual/Auto
Polarity	Black-hot/White-hot
Color Palettes	Support (1)
Image Processing	DNR
	DDE
	Histogram equalization
Image Mirror	Horizontal/Vertical/Diagonal
Power Supply(2)	
Power Supply Range	3.8～5.2VDC(3)

Typical Power Consumption @25℃	About 350mW
Interfaces(4)	
Digital Video	CDS2, CDS3
	8Bit LVCMOS, 2lane MIPI
Serial Communication Interfaces	UART(1.8V)
Temperature Measurement Performance	
Temperature Measurement Range	-20℃～+550℃
Accuracy	±3℃ or ±3% of reading, the larger value shall prevail
Physical Properties	
Weight (with 3.2mm lens)	About 6g
Size(w/o lens)	Detecting Part: 14.6mm*21mm Processing Part:21mm*21mm
Environmental Adaptation	
Operating Temperature Range	-20℃～60℃
Storage Temperature Range	-45℃～85℃
Humidity	5～95%, no condensation
Vibration	6.06g, random vibration, all axes
Shock	40g, 11ms, half sine wave, 3-axis six-direction

Note:

(1)The description of power supply and interfaces applies only to the factory state without expansion components. For detailed functions of the expansion components, refer to the User Expansion Component Manual;

(2)The voltage values here refer to the voltage at the thermal imaging core connectors;

(3)Our standard expansion components need to be equipped.

4.User Interface Descriptions

The thermal imaging module uses Hirose FH35C-39S-0.3SHW FPC connector, which includes power supply interface, serial communication interface and digital video interface. The user can connect the thermal imaging module with FPC flat cables (39pin, 0.3mm interval and the same surface). Flat cable with length of 50 mm is provided by default.

4.1 Pin Assignment and Pin Description of Hirose Connector

Table 4.1 Pin Assignment and Pin Description of Hirose Connector(1)

Pin No.	Pin Name	Function Description
1	VDD50	5V input
2	VDD50	5V input
3	VDD50	5V input
4	GND	Ground
5	GND	Ground
6	UART_RX	Serial communication interface, 1.8V
7	UART_TX	Serial communication interface, 1.8V
8	NC	Suspend
9	NC	Suspend
10	NC	Suspend
11	NC	Suspend
12	GND	Ground
13	DV0	LSB of digital signal , 1.8V
14	DV1	Digital signal, 1.8V
15	DV2	Digital signal, 1.8V
16	DV3	Digital signal, 1.8V
17	DV4	Digital signal, 1.8V
18	DV5	Digital signal, 1.8V
19	DV6	Digital signal, 1.8V
20	DV7	Digital signal, 1.8V
21	DV8	Digital signal, 1.8V
22	DV9	Digital signal, 1.8V
23	DV10	Digital signal, 1.8V
24	DV11	Digital signal, 1.8V
25	DV12	Digital signal, 1.8V
26	DV13	MSB of digital signal(14Bit), 1.8V
27	DV_Vsync	Valid signal of frame, 1.8V
28	DV_Hsync	Valid signal of line, 1.8V
29	CLK	Clock signal, 1.8V
30	GND	Ground
31	MIPI_CLK+	MIPI clock
32	MIPI_CLK-	MIPI clock

Pin No.	Pin Name	Function Description
33	GND	Ground
34	MIPI_DATA0+	MIPI data
35	MIPI_DATA0-	MIPI data
36	GND	Ground
37	MIPI_DATA1+	MIPI data
38	MIPI_DATA1-	MIPI data
39	GND	Ground

Note:

The definition of Hirose connectors applies only to the factory state without expansion components.

4.2 The Power Supply Requirements for Hirose Connectors

Table 4.2 Power Supply Requirements Description

Power Name	Supply Voltage	Max Noise	Peak Current	Steady-State Current(1)	Power Consumption(1)
MAIN_POWER	3.8V~5.2V	10mV	400mA	50mA	250mW

Note:

The steady-state current and power consumption are typical values under standard conditions at 25℃.

4.3 List of User Expansion Component

Table 4.3 Description of the Analog Video Expansion Component Interface

Model	Figure	Main Interfaces/Functions	Fitting Module
TCX2107V100F023		Power supply, typical voltage 5V Communication via RS232 Analog video output（1）	C256

Note*:*

Only image data is supported under analog video output.

4.4 Parallel Digital Video Format

Table 4.4 Description of Digital Video Format

Video Format	CDS_2[(1)]	CDS_3	LVCOMS
Supported Models	256	256	256
I/O Qty.(bit)	CLK(1) HSync(1) VSync(1) Data signal(14)	CLK(1) HSync(1) VSync(1) Data signal(8)	CLK(1) HSync(1) VSync(1) Data signal(14)
Progressive/ interlaced	Progressive	Progressive	Progressive
Clock Frequency/MHz	9.375	9.375	9.375
External Sync	Yes	Yes	Yes
Internal Reference Code	Yes	Yes	No
Data Format	RAW image +TEMP 1 CLK for 1 pixel	YUV422+TEMP 2 CLKs for 1 pixel UY first, VY follow-up Temperature: low byte first, then high byte	RAW image
Support Color Palettes/ Polarity	Color Palettes unavailable	Yes	Color Palettes unavailable
Image Data Source Selection	DRC	DRC	Support
Array Format (column×line)	512×192	1024×192	256×192

Note:

The second half of each line of CDS_2 is 14-bit temperature data;

4.4.1 CDS2 Digital Video Format

CDS2 digital video contains 1 clock signal (Clock), 1 frame valid signal (Vsync), 1 line valid signal (Hsync), and 14 data signals (DATA). The video data consists of two parts: the first half of each line is the image, a pure grayscale image with an effective bit depth of 8 bits; the second half of each line is temperature data with an effective bit depth of 14 bits.

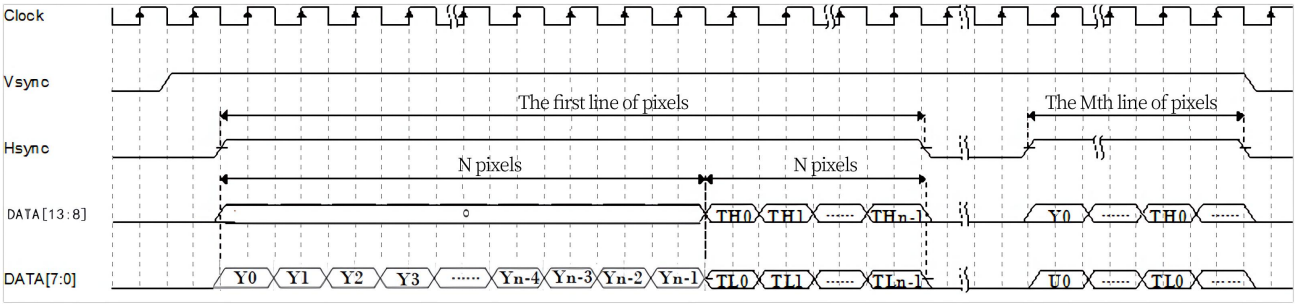

Figure 4.1 CDS2 Digital Video Timing

Note:

(1) "T" stands for temperature data (effective data bits is low 14-bit), "TH" stands for high 6-bit, and "TL" stands for low 8-bit.

(2) External synchronization signal mode is adopted. "Vsync" represents frame synchronization signal and "Hsync" represents row synchronization signal.

*(3) The output data in each row is 2 times of the array N, such as thermal camera module with array of 256*192, contains 256*2=512 clock cycles (N = 256) in each row, with 192 rows (M=192) in each frame.*

4.4.2 CDS3 Digital Video

The CDS3 digital video can output images with color palettes, the frame sync signals and line sync signals are not required for CDS3 digital video, only one CLK signal and 8 data lines are needed, and the CLK frequency is 9.375MHz.

CDS3 video data is arranged in a progressive scan format. Each line of CDS3 video data includes three parts: reference codes (EAV/SAV), blanking interval, and data region. The format of one frame of video output from the thermal imaging module is shown in the table below:

Table 4.4 The Format of One Video Frame

Reference code in invalid line EAV	Blanking Region 0x80 0x10	Reference code in invalid line EAV	Invalid data region 0x80 0x10	
Reference code in valid line EAV	Blanking Region 0x80 0x10	Reference code in valid line EAV	Valid image data 256*192 pixel/256*192*2 clk	Valid temp data 256*192 pixel/256*192*2 clk
Reference code in invalid line EAV	Blanking Region 0x80 0x10	Reference code in invalid line SAV	Invalid data area 0x80 0x10	

In above table, the reference code EAV in invalid lines in the top left corner is the start of a frame, the invalid data area in the bottom right corner is the end of a frame. There is no line sync signal or field sync signal for CDS3 video, it adopts the reference codes (SAV or EAV) to represent the start/end of a line or frame, EAV represents the start of the next line and the end of the previous line, SAV represents the start of data area in the line. Each group of reference code is corresponding to 4 CLK cycles, that is ,

each reference code includes 4 bytes, the contents of the first 3 bytes are fixed: 0xFF, 0x00 and 0x00，the content of the fourth byte depends on the position of the reference code. The contents of the fourth byte are shown in the following table:

Table 4.5 The Fourth Byte of the Reference Code

Reference Code Position	Reference Code
EAV in invalid lines	0xB6
SAV in invalid lines	0xAB
EAV in valid lines	0x9D
SAV in valid lines	0x80

The data in blanking area and data area is arranged in the order of Cb Y Cr Y, the width of Cb, Cr and Y is 8-bit and corresponds to 1 CLK cycle respectively. A group of Cb Y Cr Y is corresponding to 2-pixel data, that is 4 CLK cycles.

For blanking area and invalid data, Cb and Cr are fixed as 0x80, Y is fixed as 0x10. For image area with valid data, the chroma Cb and Cr is 8-bit, the brightness Y is 8-bit gray scale. For temp area with valid data, the chroma Cb and Cr is low 8bits of the temp data, that is TEMP [7:0], the brightness Y is high 8bits of the temp data, that is TEMP [15:8].

For the format and content of CDS3 digital video in each line, see the following figure:

Table 4.6 The Format of One Line of Video Data

	EAV reference code				Blanking region				SAV reference code				Data							
													Image				Temp			
Byte Count	4 Bytes				---				4 Bytes				256*2 Bytes				256*2 Bytes			
	FF	00	00	EVA	Cb	Y	Cr	Y	FF	00	00	SAV	Cb	Y	Cr	Y…	Cb	Y	Cr	Y…
Invalid line	FF	00	00	B6	80	10	80	10	FF	00	00	AB	80	10	80	10	80	10	80	10
Valid line	FF	00	00	9D	80	10	80	10	FF	00	00	80	Cb	Y	Cr	Y	TEMP [7:0]	TEMP [15:8]	TEMP [7:0]	TEMP [15:8]

4.4.3 LVCMOS Digital Video

LVCMOS digital video includes 1 clock signal (Clock), 1 line valid signal (Line_Valid), 1 frame valid signal (Frame_Valid), and 14 data signals (DV0-DV13). The pixel data bit depth can be either 14 bits or 10 bits. When the user selects raw data (RAW) or temperature (TMP) data, the bit depth is 14 bits, i.e., DV[13:0], where DV0 is the LSB and DV13 is the MSB. When the user selects data processed by image processing (DRC), the bit depth is 10 bits, i.e., DV[9:0], where DV0 is the LSB and DV9 is the MSB.

LVCMOS digital video can be enabled or disabled via control commands. When enabled, it is possible to select the output of raw data (ORG), non-uniformity correction (NUC) data, or image processing (DRC) data.

When image processing (DRC) data is selected, the thermal imaging module does not support digital zoom or temperature information display functions.

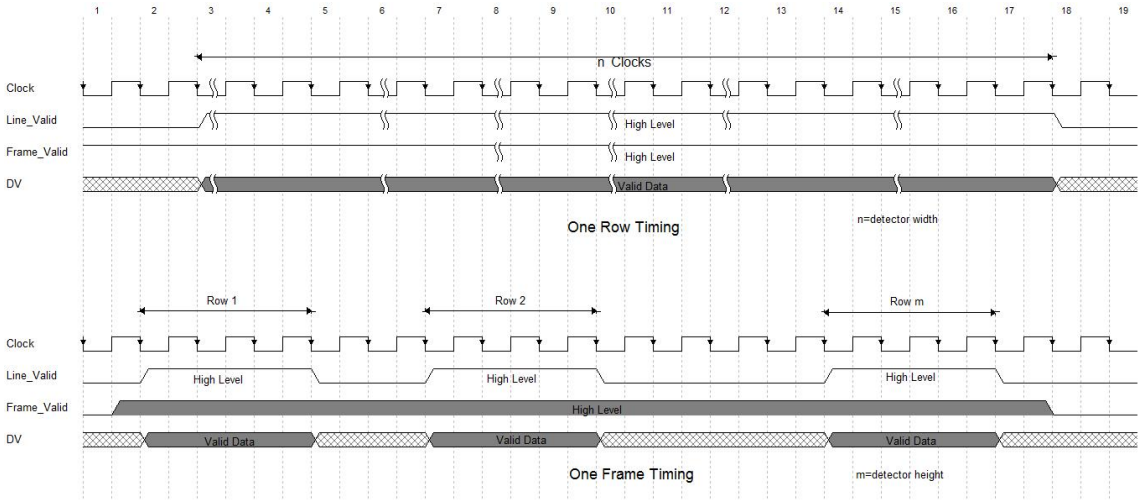

Figure 4.2 LVCMOS Digital Video Timing Diagram

Note:

(1) DV is recommended to be sampled on the rising edge of the Clock.

(2) Both Line_Valid and Frame_Valid are active-high signals.

(3) *After Line_Valid is asserted, it remains active for n Clock cycles, corresponding to the validity of data from the first to the last column of the line.*

4.5 MIPI protocol

4.5.1MIPI Protocol Overview

This product uses a 2-lane MIPI interface, which includes 1 pair of source-synchronous differential clock signals and 2 pairs of differential data lines.

The clock signal switches to high-speed mode at the start of each frame and exits high-speed mode at the end of each frame. Between frames, it operates in low-power mode (with both data and clock lines at a high level of 1.2V). The clock frequency used in this product is 218 MHz.

At the start of each frame, the data lines send a frame start packet, and at the end of the frame, they send a frame end packet. Between the frame start and end packets, there are data long packets

corresponding to the height of the image array (for a 256*192 module, there are 192 long packets in total). Each long packet contains one row of valid data.

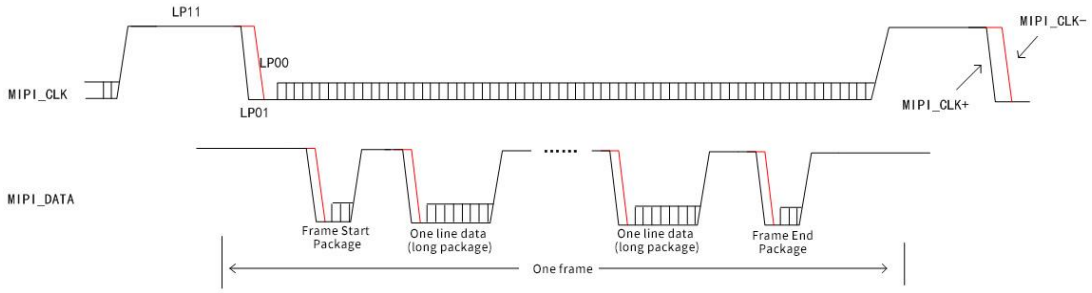

Figure 4.3 Schematic of One Frame of Data

4.5.2 Module Output Description

After powering on, the camera module starts outputting MIPI digital video, which includes image and temperature data. The array format is 1024x192, and each frame contains (256*2)x192×16-bit data. The clock frequency is 218 MHz, and the data is transmitted over 2 lanes. The data format is set to RAW8 (standard MIPI CSI-2 protocol), requiring the backend to assemble it into 16-bit data, with the lower byte first.For each line of valid data, the first 256×16-bit are image data (if pseudo-color is used, UV first, then Y, UYVY), and the next 256×16-bit are temperature data, as shown in the diagram below.

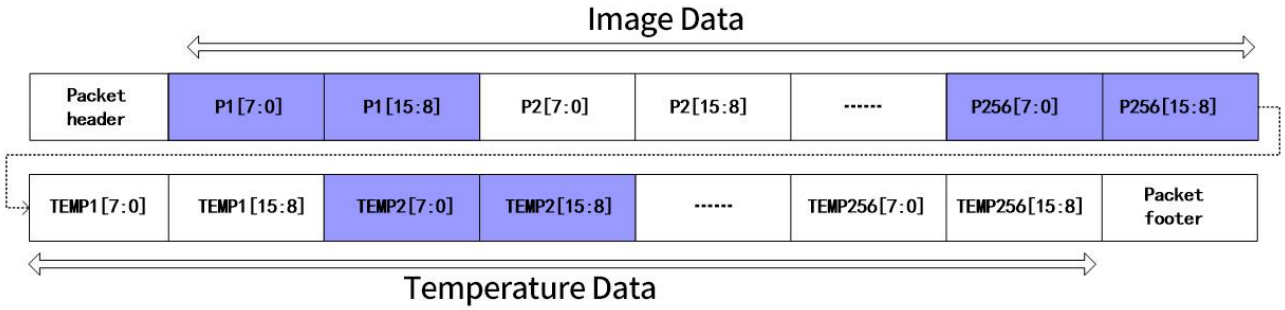

Figure 4.4 The illustration of a line of valid data

5.Structural Drawings

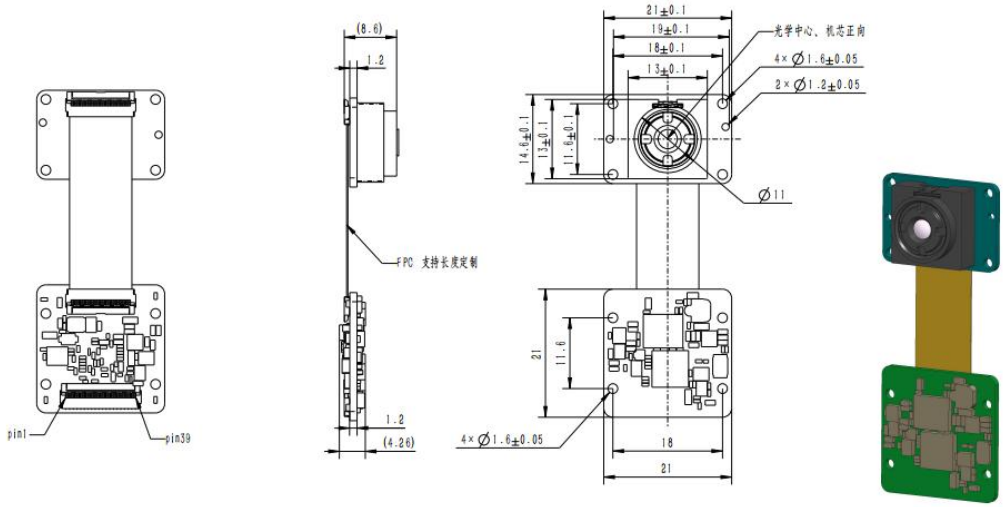

Figure 5.1 Module Dimensions(With 3.2mm,F1.1 Lens)

The size of the camera module varies with different lenses and expansion components. Please refer to the detailed camera module dimensions diagram for more information.

6.Cautions

To protect you and others from injury or to protect your equipment from damage, please read all the following information before using your equipment.

1. The product shall not face towards the sun or other high-intensity radiation sources directly;
2. The ideal environment temperature for operating is - 20 ℃ to 60 ℃;
3. The lens shall not be touched or hit with hands or other objects;
4. The equipment and cables shall not be touched with wet hands;
5. Please do not bend or damage cables;
6. Scrubbing your equipment with diluents is prohibited;
7. Do not unplug and plug cables when the power is on;
8. Wrong cable should not be connected in case that brings damages to the equipment;
9. Please pay attention to prevent static electricity;
10. Please do not disassemble the equipment. If there is any fault, please contact us, and professional personnel will carry out maintenance.